Multichannel DDS controller manual

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The multichannel DDS controller (i.e. DDS box) is a circuit which provides direct access to four Analog Devices AD9910 evaluation boards for use in the laboratory. The AD9910 is a DDS (direct digital synthesizer) integrated circuit providing up to 400 MHz analog output. Each AD9910 chip is capable of storing up to eight preset single-tone settings called profiles which are accessible through fast switching of its profile pins. The chip has a digital ramping capability which enables controlled sweeping of the frequency, amplitude, or phase of the output.

The four AD9910 evaluation boards constitute four independent and fully accessible channels of the DDS box. The box is controlled by a single USB interface and a set of external control pins which offer real-time access to the evaluation boards’ profile selection and ramping functions. A LabVIEW control program handles communication to the box from a PC. Unused channels may be externally powered down by front-panel switches or in software.

Other features of the AD9910 which are not yet accessible in this implementation but which may be incorporated in future DDS box versions include:

- RAM modulation mode, a function for generating arbitrary time dependent waveforms of amplitude, frequency, or phase using 1024 available words of 32-bit RAM,
- output shift keying, a function enabling internal or external amplitude modulation of the chip’s output,
- parallel data port modulation mode, a function for arbitrary fast control of the chip’s output using the 18-bit parallel data port,
- and synchronization of multiple boards.
This document is divided into three parts: a user manual, a hardware manual, and a programming manual. The user manual provides instructions for the setup and basic use of the DDS box. The hardware manual explains how to construct a DDS box and provides information about its component parts. The programming manual describes the current LabVIEW programming interface for the DDS box. The programming interface consists of a set of low-level driver VIs which access the basic functions of the AD9910 chip. This programming interface can be incorporated into existing LabVIEW programs to add DDS functionality.

Quick Specifications

Output frequency 0 MHz to 400 MHz

Output power 0 dBm to -70 dBm (approx)

Power supply 5 V DC (max current draw 1.7 A, min current draw 0.5 A)
Part I

User’s manual
1 External connections

**Power connections** The DDS box is powered by a single 5 V DC supply. The peak continuous current drawn will not exceed 2 A. Connect the 5 V and ground supplies via banana cables.

**RF outputs** The RF output signals from each of the four channels are accessible via SMA connectors on the front panel. The output from any powered-down channel may be left unconnected.

**USB control** The DDS box connects to its control computer through the USB type B socket on the front panel.

**I/O connections** 20 additional input TTL control pins are accessible via the ribbon cable connector on the front panel. These pins safely accept both 5 V and 3.3 V logic. They are all passively pulled to ground, so when they are not in use, they may be left unconnected (this is the case when the only needed function for all channels is that of a constant single-tone RF generator). These pins provide real-time access to the profile switching and the ramp control functions of each channel. See figure 1.1 for the pin-out diagram and chapter 2 for information on using these features.
Figure 1.1: Pin-out diagram of the ribbon connector socket for the front panel TTL inputs
2 Operating procedures

2.1 Turning on the box

Apply 5 V power to the DDS box, and run a USB cable between the box and the control computer.\(^1\) The green LED on the USB interface should blink when it is ready to use. Ensure that all channels are switched to the on state before initializing the box using the LabVIEW interface.

2.2 Setting calibration values

The accuracy of frequencies generated by the DDS channels depends on accurate knowledge of the reference clock frequencies. Slight deviations of the (nominally 1 GHz) reference frequencies can be calibrated out of each channel by supplying the known frequency values of the four oscillators. If the exact clock frequencies are not known, they may be determined in situ by using the following procedure on each channel:

1. Set the calibration reference clock frequency to 1000 MHz.

2. Set the channel to generate a 250 MHz single-tone frequency.

3. Measure the precise value of the output frequency.

4. Set the calibration reference clock frequency to \(4 \times \) the measured frequency.

\(^1\)When connecting the USB interface to a computer for the first time, allow the operating system to detect the new device, then follow the on-screen instructions to install the needed drivers (National Instruments Measurement & Automation Explorer must be installed for this to work properly).
The accuracy of the output RF power generated by the channels depends on prior knowledge of the full-scale output power. To set this calibration do the following for each channel:

1. Set the calibration full-scale output power to 0 dBm.
2. Set the channel to generate a single-tone RF output with power greater than or equal to 0 dBm.
3. Measure the precise value of the output power.
4. Set the calibration full-scale output power to the measured power.

2.3 Generating a constant single-tone output

With the profile control pins of the desired channel disconnected or set to logic zero, load the RF generation parameters (frequency, amplitude, and phase offset) into the channel’s profile zero register using the LabVIEW interface. The channel’s RF output will immediately reflect the change in settings.

2.4 Switching between multiple single-tone profiles

A single DDS channel may store up to eight single-tone profiles at one time. To enable fast switching between these profiles, load the RF generation parameters (frequency, amplitude, and phase offset) into the desired profiles. The channel’s RF output will immediately reflect the settings specified by the external logic supplied to profile control pins on the box’s front panel (see figure 1.1). The profile control pins for each channel labeled PO, P1, and P2 encode bits 0, 1, and 2, respectively, of the currently active profile number as table 2.1 shows explicitly. Use positive logic (either 3.3 V or 5 V) to set the profile pins.

2.5 Performing a frequency, amplitude or phase ramp

Digital ramp generation is a mode of the AD9910 chip in which a single RF generation parameter (frequency, amplitude or phase offset) is linearly ramped (increased or decreased) as a function of time. The ramp may be continuous like a triangle ramp, or it may be set to wait for an external trigger. Both the rising and falling slopes of the ramp may be specified independently. Only the data for a single parameter ramp may be stored at one
Table 2.1: Profile pin logic settings

<table>
<thead>
<tr>
<th></th>
<th>P2</th>
<th>P1</th>
<th>P0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Profile 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Profile 1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Profile 2</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Profile 3</td>
<td>0</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Profile 4</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Profile 5</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Profile 6</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Profile 7</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

time (i.e. there are not multiple “ramping profiles” that may be stored and accessed later the manner of single-tone profiles). Whenever one parameter is being ramped, the other two parameters are given by the currently active single-tone profile.

To perform a digital ramp first ensure that the channel’s currently active single-tone profile has the desired static parameters. Then load into the channel the desired ramp generation parameters (the parameter to ramp, the limits and duration of the ramp, and the ramping pattern), and enable ramping using the LabVIEW software. Depending on the ramping pattern and the state of the DRCTL pin, the output parameter may begin ramping immediately from the low limit to the high limit, or else it will jump to the initial state and wait for a trigger to initiate the ramp. If a command to clear the digital ramp accumulator is sent from the software anytime during digital ramp generation mode, it effectively causes the ramping pattern to be reset to its initial state. The relevant front-panel control pins for ramping are the DRCTL pins (see figure 1.1). The following is a description of the four possible ramping patterns.

**Normal ramp**

*Normal ramp* is a manually triggered mode. The initial state of the ramp generator in this mode is always the lower ramp limit. If the DRCTL pin is initially active, the positive ramp will begin immediately. Otherwise, a low-to-high transition on DRCTL initiates the positive ramp. When the ramp output reaches the upper limit, it will remain at that value until the next high-to-low transition on DRCTL, at which point it will begin the negative ramp. When the lower limit is reached, the positive ramp can be restarted with another
low-to-high transition on DRCTL and so on. See figure 39 on the AD9910 data sheet for more information about normal ramp generation.

**No-dwell high**

*No-dwell high* is a manually triggered mode. The initial state of the ramp generator in this mode is the lower ramp limit. In this mode the ramp generator output is analogous to a sawtooth wave where the rising edge of the sawtooth is triggered by a low-to-high transition on DRCTL. When triggered, the output of the ramp generator will rise to the upper ramp limit, at which point it will immediately snap back to the lower ramp limit to await another trigger. See figure 40 on the AD9910 data sheet for more information about no-dwell ramp generation.

**No-dwell low**

*No-dwell low* mode is similar to *no-dwell high* mode except for the following differences. The output of the ramp generator is initially at the upper ramp limit. When triggered by a high-to-low transition on DRCTL, the output will ramp to the lower ramp limit, at which point it will immediately snap back to the upper ramp limit to await another trigger.

**Continuous ramp**

In *continuous ramp* mode the output of the ramp generator starts at the lower ramp limit and automatically oscillates between the two limits. In this mode the direction of the ramp can be changed midway through its progress, if desired, by toggling the DRCTL pin: a high-to-low transition on DRCTL will cause the output to “reverse” a positive ramp by beginning a negative ramp from the current output value. Likewise, a low-to-high transition on DRCTL will cause the output to begin a positive ramp from its current value.

### 2.6 Powering down channels and restarting them

Channels can be externally powered down simply by flipping the front-panel switches to external power-down mode. This disables communication to the AD9910, however, so it should not be done during initialization of the channel. The channel will return to its previous state when the channel’s front-panel switch is returned to the *on* position.
A more complete power-down state can be achieved by issuing a power-
down command to the channel in software. This internal power-down state
disables more subsystems of the AD9910 chip, allowing the channel to draw
minimum current.\(^2\) Note that in an internal power-down state, serial com-
munication is not disabled. The channel will return to its previous state when
a wake-up command is issued in software. Note that in either power-down
state no information uploaded to the chip since its last re-initialization will
be lost.

### 2.7 Turning off the box

Before turning off the DDS box, be sure to properly stop or close out the Lab-
VIEW program that initialized it. This is to prevent memory leaks due to an
open device reference. The box can be safely turned off by disconnecting its
5 V power supply. The USB interface may remain connected to the computer;
it is powered by the USB line, so it will remain on as long at it is plugged in.

\(^2\)When all channels are set to their internal power-down states, the 0.5 A current draw of
the box is dominated by the reference clocks which are not disabled.
3 Troubleshooting

Here is a list of potential problems presented with possible solutions. Solutions are offered roughly in order of likelihood.

**Problem** The DDS box does not respond to program commands.

1. Make sure that the channel being used is not switched to external power-down mode (front-panel switch).
2. Check the DDS board power supplies.
3. Check that the channel’s data wires are securely connected to DDS board.
4. Check that power is being supplied to the IO board and that IO Update signals are getting through the OR gates to the DDS boards.
5. Make sure the jumpers on all of the DDS boards are set properly.
6. Reset the NI USB-8451 interface by first turning off the box, then unplugging the USB from the computer and plugging it back in. The green LED on the interface should blink when it is plugged in and ready to use.

**Problem** No RF output.

1. Make sure that the channel being used is not switched to external power-down mode (front-panel switch).
2. Make sure that the channel is set to a profile for which the amplitude and frequency values specified in the LabVIEW control software are non-zero.
3. Check the DDS board power supplies.
4. Check that the channel’s data wires are securely connected to DDS board.

5. Check that power is being supplied to the IO board and that IO Update signals are getting through the OR gates to the DDS boards.

6. Check the power to the 1 GHz reference oscillators on the clock board. The board has one 3.3 V voltage regulator for power and another 1.65 V regulator providing a voltage reference.

7. Check the output of the reference clock by turning off the box, unplugging the SMA cable running from the clock board to the CLK INPUT port on the channel’s DDS board, and observing the signal with a frequency counter or spectrum analyzer. The clock signal should have a single 1 GHz frequency component with amplitude of about ?? dBm and no phase noise above ?? dB below the main peak.

**Problem** The output has an unusual amount of amplitude or phase noise.

1. Check the DDS board power supplies.

2. Check the power to the 1 GHz reference oscillators on the clock board. The board has one 3.3 V voltage regulator for power and another 1.65 V regulator providing a voltage reference.

3. Check the output of the reference clock by turning off the box, unplugging the SMA cable running from the clock board to the CLK INPUT port on the channel’s DDS board, and observing the signal with a frequency counter or spectrum analyzer. The clock signal should have a single 1 GHz frequency component with amplitude of about ?? dBm and no phase noise above ?? dB below the main peak.

**Problem** The box draws a lot of current (over 1 A) even when all of the channels are externally switched to power-down mode. Note that about 0.7 A is not unusual.

1. Make sure the jumpers on all of the DDS boards are set properly.

2. Look for short circuits.
Part II

Hardware manual
4 Circuit boards

The DDS box contains three circuit boards in addition to the four AD9910 evaluation boards and the USB interface. These are the I/O interface board, the power supply board, and the clock board. These three boards take their 5 V and ground supplies directly from the case. See chapter 6 for details about the connections between boards.

The I/O interface board takes input logic signals from the USB interface, the front panel switches, and the additional logic inputs. It buffers them where necessary and sends them to an output ribbon cable which splits off to various digital logic pins on the four evaluation boards. Note that for each channel IO update signals may come from either the USB interface or the front panel, so the IO update signal sent to the boards is the logical OR of these two input sources. The electrical schematic and board design are shown in figures 4.1 and 4.2 respectively.

The power supply board provides power for the evaluation boards. For optimal performance each evaluation board requires two separately regulated 3.3 V and two separately regulated 1.8 V DC power sources. 16 low drop-out voltage regulators provide these sources which are supplied to the four evaluation boards through an output ribbon cable. The electrical schematic and board design are shown in figures 4.3 and 4.4 respectively.

The clock board provides stable 1 GHz reference frequencies to each evaluation board. The AD9910 derives both its internal logic clock and its RF output from its reference clock input. Although each AD9910 evaluation board is capable of generating this 1 GHz reference via an on-board quartz oscillator and phase-locked-loop (PLL), experience has shown that phase noise and stability are greatly improved by using an external reference. The four 1 GHz output signals of the clock board are sent to the CLK INPUT ports of the evaluation boards via SMA cables. The electrical schematic and board design of the clock board are shown in figures 4.5 and 4.6 respectively.
Figure 4.1: I/O board electrical schematic
Figure 4.2: I/O board design
Figure 4.3: Power supply board electrical schematic
Figure 4.4: Power supply board design
Figure 4.5: Clock board electrical schematic
Figure 4.6: Clock board design
5 Hardware

5.1 External hardware

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<thead>
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<th>Quantity</th>
<th>Item</th>
<th>Description</th>
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</thead>
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<tr>
<td>1</td>
<td>enclosure</td>
<td>rack mount: 17.5 in. wide by 12 in. deep (or similar)</td>
</tr>
<tr>
<td>4</td>
<td>switches</td>
<td>SPST toggle (for external power-down)</td>
</tr>
<tr>
<td>1</td>
<td>ribbon connector</td>
<td>20 pin male panel mount (for external IO connections)</td>
</tr>
<tr>
<td>2</td>
<td>banana sockets</td>
<td>for 5 V and ground power supplies</td>
</tr>
<tr>
<td>1</td>
<td>5 V cooling fan</td>
<td>Copal Electronics F251R-05LLC (or similar)</td>
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5.2 Electronics

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Item</th>
<th>Description</th>
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<tbody>
<tr>
<td>4</td>
<td>AD9910 evaluation boards</td>
<td></td>
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<tr>
<td>1</td>
<td>NI USB-8451</td>
<td>USB to serial communication interface</td>
</tr>
<tr>
<td>1</td>
<td>I/O board</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Power supply board</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Clock board</td>
<td></td>
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</table>
### I/O board components

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Type</th>
<th>Value</th>
<th>Parts</th>
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<tbody>
<tr>
<td>1</td>
<td>regulator</td>
<td>MC33269T-3.3</td>
<td>IC1</td>
</tr>
<tr>
<td>1</td>
<td>IC</td>
<td>74LS32N</td>
<td>IC2</td>
</tr>
<tr>
<td>3</td>
<td>IC</td>
<td>SN74LVC245A</td>
<td>IC3–IC5</td>
</tr>
<tr>
<td>20</td>
<td>resistor</td>
<td>10 k</td>
<td>R1–R20</td>
</tr>
<tr>
<td>1</td>
<td>capacitor</td>
<td>1 uF</td>
<td>C1</td>
</tr>
<tr>
<td>1</td>
<td>capacitor</td>
<td>10 uF</td>
<td>C2</td>
</tr>
<tr>
<td>4</td>
<td>capacitor</td>
<td>0.01 uF</td>
<td>C3–C6</td>
</tr>
<tr>
<td>1</td>
<td>male header</td>
<td>2×17 pin</td>
<td>JP1</td>
</tr>
<tr>
<td>1</td>
<td>male header</td>
<td>2×24 pin</td>
<td>JP2</td>
</tr>
<tr>
<td>1</td>
<td>male header</td>
<td>2×30 pin</td>
<td>JP3</td>
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### Power supply board components

<table>
<thead>
<tr>
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<th>Type</th>
<th>Value</th>
<th>Parts</th>
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</thead>
<tbody>
<tr>
<td>8</td>
<td>regulator</td>
<td>MSP1825S-3.3</td>
<td>IC1–IC8</td>
</tr>
<tr>
<td>8</td>
<td>regulator</td>
<td>MSP1825S-1.8</td>
<td>IC9–IC16</td>
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<td>capacitor</td>
<td>1 uF</td>
<td>C1–C32</td>
</tr>
<tr>
<td>1</td>
<td>male header</td>
<td>2×20 pin</td>
<td>JP1</td>
</tr>
<tr>
<td>1</td>
<td>male header</td>
<td>1×3 pin</td>
<td>JP2</td>
</tr>
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</table>

### Clock board components

<table>
<thead>
<tr>
<th>Quantity</th>
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<th>Value</th>
<th>Parts</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>oscillator</td>
<td>FVXO-LC73</td>
<td>IC1–IC4</td>
</tr>
<tr>
<td>1</td>
<td>regulator</td>
<td>MC33269T-3.3</td>
<td>IC5</td>
</tr>
<tr>
<td>1</td>
<td>regulator</td>
<td>LD1086V</td>
<td>IC6</td>
</tr>
<tr>
<td>4</td>
<td>resistor</td>
<td>100 ohm</td>
<td>R1–R4</td>
</tr>
<tr>
<td>1</td>
<td>resistor</td>
<td>237 ohm</td>
<td>R5</td>
</tr>
<tr>
<td>1</td>
<td>resistor</td>
<td>76.8 ohm</td>
<td>R6</td>
</tr>
<tr>
<td>4</td>
<td>capacitor</td>
<td>0.01 uF</td>
<td>C1–C4</td>
</tr>
<tr>
<td>1</td>
<td>capacitor</td>
<td>1 uF</td>
<td>C5</td>
</tr>
<tr>
<td>3</td>
<td>capacitor</td>
<td>10 uF</td>
<td>C6–C8</td>
</tr>
<tr>
<td>1</td>
<td>male header</td>
<td>1×2 pin</td>
<td>JP1</td>
</tr>
<tr>
<td>4</td>
<td>female SMA jack</td>
<td></td>
<td>X1–X4</td>
</tr>
</tbody>
</table>
6 Assembling the box

The following sections give detailed instructions on the assembly of a DDS box. See figure 6.1 for a suggested box layout. Attention should be paid to minimizing clutter by keeping wires short and bundling them where appropriate. While the DC regulators on the power supply board have not shown excessive heating, it is suggested to place the power supply board next to the cooling fan in an orientation that allows air to flow between the regulators before being exhausted from the box. Several holes in the side of the box opposite the fan will suffice for ventilation.

Make appropriate labels for the front panel components. Each of the four channels has an SMA jack labeled RF OUT and a toggle switch with labels ON and PWR DN. Note that when the switch is in the on position (high) the center pin connects to ground, and when it is in the power-down position (low) the center pin connects to 3.3 V. Label the exposed USB socket of the NI USB-8451 USB. Label the male ribbon connector socket I/O connections. The user should refer to chapter 1 for the pin-out of this connector. Label the two banana cable connectors 5 V and GND.

6.1 Preparing the boards

Refer to chapters 4 and 5 for diagrams and parts-lists for assembling the I/O, power supply, and clock boards. Note that all double-row header pins on the boards may be replaced with male ribbon connector sockets if available. This simplifies the process of connecting boards; just ensure that the orientation of the connector is correct before soldering. It may be practical to make the ribbon cables ahead of time to use as a reference (see section 6.2).
6.2 Making electrical connections

The three home-made boards act as an electrical interface between the four evaluation boards and the outside world (the RF output is the only direct connection between the evaluation boards and the case). This serves both to compartmentalize the design and to protect the evaluation boards from accidental misuse (while the components of the home-make boards can be easily replaced, the evaluation boards can not). Table 6.1 gives the details of each electrical connection. Refer to figures 6.2 through 6.4 for the header pin assignments.

6.3 Setting the evaluation board jumpers

Each AD9910 evaluation board has a set of jumpers which controls its mode of communication. The factory setting of these jumpers enables communi-
Table 6.1: DDS box electrical connections

<table>
<thead>
<tr>
<th>Qty</th>
<th>Type</th>
<th>Termination 1</th>
<th>Termination 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>34 wire straight ribbon</td>
<td>NI USB-8451</td>
<td>I/O board JP1</td>
</tr>
<tr>
<td>1</td>
<td>≥48 wire straight ribbon</td>
<td>I/O board JP2</td>
<td>eval. board logic pins (via individual crimp connectors)</td>
</tr>
<tr>
<td>1</td>
<td>34 wire straight ribbon</td>
<td>I/O board JP3</td>
<td>front panel (switches, pwr supplies, I/O ribbon connector)</td>
</tr>
<tr>
<td>1</td>
<td>40 wire twisted-pair ribbon</td>
<td>power supply board JP1</td>
<td>eval. board power supply pins</td>
</tr>
<tr>
<td>2</td>
<td>wire</td>
<td>front panel power supplies</td>
<td>power supply board JP2</td>
</tr>
<tr>
<td>2</td>
<td>wire</td>
<td>front panel power supplies</td>
<td>clock board JP1</td>
</tr>
<tr>
<td>4</td>
<td>SMA (rt-angle to rt-angle)</td>
<td>clock board outputs</td>
<td>eval. board CLK INPUT (J1) ports</td>
</tr>
<tr>
<td>4</td>
<td>SMA (rt-angle to bulkhead)</td>
<td>eval. board FILTERED IOUT (J4) port</td>
<td>front panel</td>
</tr>
<tr>
<td>4</td>
<td>jumper (or short wire)</td>
<td>eval. board DRHOLD logic pin</td>
<td>neighboring eval. board ground pin</td>
</tr>
</tbody>
</table>
CHAPTER 6. ASSEMBLING THE BOX

V_in from case (+5 V)
Gnd from case
Toggle switch 1 low connection
Toggle switch 2 low connection
Toggle switch 3 low connection
Toggle switch 4 low connection
Toggle switch 1 center
Toggle switch 3 center
Toggle switch 2 center
Toggle switch 4 center
Channel 1 P0
Channel 1 P1
Channel 1 P2
Channel 1 DRCTL
JP3
1 31 11 21
34 30 20 10
Gnd
Gnd
Gnd
Gnd
Channel 1 IO UPDATE

To make ribbon cable socket mounted on case
Connect the two ribbon connectors so that pins 1-20 on the front panel correspond to pins 15-34 on JP3.

Wire pins from JP2 to the corresponding labelled pins on the four DDS evaluation boards.

Figure 6.2: I/O board header pin assignments

NI USB-8451 physical connections

Front panel I/O connections
Connect the pins of JP1 on the power supply board to each of the labeled evaluation board power supplies by clamping the bare wire ends into the contacts. Ignore unused ground pins.

Figure 6.3: Power supply board header pin assignments

Connect the clock board power supply pins to the case power supply (5 V and GND).

Figure 6.4: Clock board header pin and SMA jack assignments
cation via an on-board USB connection which interfaces with the AD9910 chip through an on-board field-programmable gate array (FPGA). Analog Devices ships a control program with graphical user interface (GUI) that uses this mode of communication. Since the DDS box has its own serial communication interface, this USB and FPGA circuitry must be bypassed on each evaluation board. To do this use the following jumper settings:

W1: set to disable
W2: set to disable
W3: remove
W4: set to disable
W5: remove
W6: remove

Also ensure that the following factory standard jumper settings have not been changed:

W7: set to REF_CLK
W11: no connection
There are currently three unused logic lines from the USB-8451 (they are the unused chip select pins). This is enough to provide a chip select, master reset, and IO update signal to an additional fifth channel if this is desired in the future. Doing so would require straightforward modifications to the other boards in the DDS box and would also require a larger enclosure. Increasing the number of channels per box beyond five would require a different solution for serial communication than is currently provided by the NI USB-8451.

Modifying the DDS box to take advantage of the parallel data port modulation mode of the AD9910 will require the addition of 18 parallel data lines per channel. The I/O board may be modified to buffer these lines for the protection of the evaluation boards, or for convenience, they may be attached directly to the case. For timing purposes it will also be necessary to access each board’s TxENABLE input and/or PDCLK output.
Part III

Programming manual
8 LabVIEW programming interface

**Note for programmers:** as of August 2011 there is a bug in the National Instruments software which prevents VIs containing NI USB-8451 drivers from being launched directly from the LabVIEW project explorer window. There is a fix available in the National Instruments KnowledgeBase: see document ID 4IPG7TJL.

### 8.1 Type definitions

**AD9910 registers**

An enum containing the AD9910 register names.

**DDS box device reference**

A cluster containing data unique to a particular DDS box. It is used for identification and also contains calibration data. All of the top-level VIs take a DDS box device reference as input and return it as output. The cluster contains:

- **NI USB-8451 device reference** A unique handle for the USB-8451 (all available units will be listed as options when plugged in to the computer)
- **DIO port** Port number for the DIO lines (set to zero)
- **Serial Clock Rate** Sets the data transfer rate (in kHz) between the computer and USB-8451 (nominally 1000 kHz)
- **Channels Settings** An array containing calibration parameters for the four DDS channels. These consist of the reference clock rates (in MHz) and
CS pin  Assignment
---  ----------------------------------
CS0  IO reset (all channels)
CS1  Channel 4 chip select
CS2  Channel 3 chip select
CS3  Channel 2 chip select
CS4  Channel 1 chip select
CS5  (unassigned)
CS6  (unassigned)
CS7  (unassigned)

Table 8.1: NI USB-8451 CS pin assignments

the full-scale output power values (in dBm) of the channels. The reference clock rate is the measured frequency of a channel’s external oscillator on the clock board (nominally 1 GHz). The full-scale output power is the measured output RF power of the channel with its output amplitude set to maximum (nominally 0 dBm).

**DDS CS pins**

An enum containing the pin assignments of the USB-8451 chip select pins (see table 8.1). The values of the enums correspond to the USB-8451 CS pin number and the names of the enums indicate the associated channel number and AD9910 pin of the assignment.

**DDS DIO pins**

An enum containing the pin assignments of the USB-8451 digital I/O (DIO) pins (see table 8.2). The values of the enums correspond to the USB-8451 DIO pin number and the names of the enums indicate the associated channel number and AD9910 pin of the assignment.

**Digital ramping pattern**

An enum containing the possible ramping patterns for digital ramp generation mode.
### DIO line Assignment

<table>
<thead>
<tr>
<th>DIO line</th>
<th>Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>P0.0</td>
<td>Channel 4 master reset</td>
</tr>
<tr>
<td>P0.1</td>
<td>Channel 3 master reset</td>
</tr>
<tr>
<td>P0.2</td>
<td>Channel 2 master reset</td>
</tr>
<tr>
<td>P0.3</td>
<td>Channel 1 master reset</td>
</tr>
<tr>
<td>P0.4</td>
<td>Channel 1 IO update</td>
</tr>
<tr>
<td>P0.5</td>
<td>Channel 2 IO update</td>
</tr>
<tr>
<td>P0.6</td>
<td>Channel 3 IO update</td>
</tr>
<tr>
<td>P0.7</td>
<td>Channel 4 IO update</td>
</tr>
</tbody>
</table>

Table 8.2: NI USB-8451 DIO line pin assignments

### 8.2 Top-level VIs

#### DDS Close

<table>
<thead>
<tr>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs</td>
<td></td>
</tr>
<tr>
<td>DDS ref in</td>
<td>DDS box device reference</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
</tr>
<tr>
<td>Outputs</td>
<td></td>
</tr>
<tr>
<td>DDS ref out</td>
<td>DDS box device reference</td>
</tr>
<tr>
<td>error out</td>
<td>error cluster</td>
</tr>
</tbody>
</table>

Disables the SPI interface and sets the TTL lines to a high-impedance state then closes the USB-8451 device reference. To save computer resources this VI must be run to close out any open device before exiting the LabVIEW program.

#### DDS Com Check

<table>
<thead>
<tr>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs</td>
<td></td>
</tr>
<tr>
<td>DDS ref in</td>
<td>DDS box device reference</td>
</tr>
<tr>
<td>channel number</td>
<td>unsigned byte</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
</tr>
<tr>
<td>Outputs</td>
<td></td>
</tr>
<tr>
<td>DDS ref out</td>
<td>DDS box device reference</td>
</tr>
<tr>
<td>error out</td>
<td>error cluster</td>
</tr>
</tbody>
</table>

Checks that serial communication with the specified channel is not interrupted. This assumes the channel is already initialized (an uninitialized channel will fail).
DDS Disable Digital Ramp

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref in</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>channel number</td>
<td>unsigned byte</td>
<td>the affected channel (1–4)</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

Disables digital ramping for the given channel, returning the channel to single-tone mode.

DDS Initialize

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref in</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

Initializes the entire DDS box by enabling the SPI communication interface, initializing the states of the DIO lines, and initializing the channels by calling DDS Re-initialize One Channel on each. This requires that all channels be powered-on and that the external power down pins not be set. This is intended to be a one-time initialization since it causes a hard reset on all channels at once. Any channel that is disabled at the time of this VI call may be initialized later, if necessary, with an individual call to DDS Re-initialize One Channel.

DDS Power Down

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref in</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>channel number</td>
<td>unsigned byte</td>
<td>the channel (1–4) to power-down</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

Sets a single channel to an internal power-down state. This is a more effective power-saving state than can be achieved by simply turning off an
active channel using its external power down pin. This VI does not affect any other data in the memory of the AD9910, so a subsequent call to DDS Wake Up will immediately return the channel to its previous state. A re-initialization of the channel or entire box will also clear the power-down state.

**DDS Re-initialize One Channel**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref in</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>channel number</td>
<td>unsigned byte</td>
<td>the channel (1–4) to initialize</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Outputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref out</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>error out</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

Resets and re-initializes the AD9910 registers for the specified channel. This clears all user data uploaded to the chip since the last initialization. The channel must not be in power-down mode at the time of this VI call.

**DDS Read Register**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref in</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>channel number</td>
<td>unsigned byte</td>
<td>the channel (1–4) to read from</td>
</tr>
<tr>
<td>register</td>
<td>AD9910 registers</td>
<td>the register to read</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Outputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref out</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>read data</td>
<td>1-D array of unsigned byte</td>
<td>the register contents</td>
</tr>
<tr>
<td>error out</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

Reads the current value of the specified register in the specified channel. Note that when reading the contents of single-tone profile registers, only the profile register currently selected by the external profile pins can be read.
### DDS Set Amplitude Ramp

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref in</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>channel number</td>
<td>unsigned byte</td>
<td>the channel (1–4) to set</td>
</tr>
<tr>
<td>ramping pattern</td>
<td>Digital ramping pattern</td>
<td></td>
</tr>
<tr>
<td>high amplitude</td>
<td>double</td>
<td>ramp upper limit amplitude in dBm</td>
</tr>
<tr>
<td>low amplitude</td>
<td>double</td>
<td>ramp lower limit amplitude in dBm</td>
</tr>
<tr>
<td>positive amplitude step</td>
<td>double</td>
<td>increasing amplitude step (stated as a fraction of the total output amplitude)</td>
</tr>
<tr>
<td>negative amplitude step</td>
<td>double</td>
<td>decreasing amplitude step (stated as a fraction of the total output amplitude)</td>
</tr>
<tr>
<td>pos ramp step time</td>
<td>double</td>
<td>increasing step time in µs</td>
</tr>
<tr>
<td>neg ramp step time</td>
<td>double</td>
<td>decreasing step time in µs</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
<tr>
<td>Outputs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDS ref out</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>error out</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

Prepares the specified DDS channel for a ramp of the amplitude of the RF output by loading the specified ramp generation parameters and enabling the ramp with amplitude set as the destination parameter. The frequency and phase offset parameters are determined by the currently active single-tone profile. It should be noted that while an effort has been made to keep all the RF amplitudes in units of dBm (decibels with respect to 1 mW output power) where possible, the amplitude ramp generated by the chip is intrinsically linear in the output current. Therefore the ramp is nonlinear in the output RF power given in either mW or in dBm. This aspect of the digital ramp generator cannot be changed, but arbitrary waveforms of amplitude could in principle be generated using the AD9910’s RAM modulation mode.
### DDS Set Frequency Ramp

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref in</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>channel number</td>
<td>unsigned byte</td>
<td>the channel (1–4) to set</td>
</tr>
<tr>
<td>ramping pattern</td>
<td>Digital ramping pattern</td>
<td></td>
</tr>
<tr>
<td>high frequency</td>
<td>double</td>
<td>ramp upper limit frequency in MHz</td>
</tr>
<tr>
<td>low frequency</td>
<td>double</td>
<td>ramp lower limit frequency in MHz</td>
</tr>
<tr>
<td>positive frequency step</td>
<td>double</td>
<td>increasing step frequency in MHz</td>
</tr>
<tr>
<td>negative frequency step</td>
<td>double</td>
<td>decreasing step frequency in MHz</td>
</tr>
<tr>
<td>pos ramp step time</td>
<td>double</td>
<td>increasing step time in µs</td>
</tr>
<tr>
<td>neg ramp step time</td>
<td>double</td>
<td>decreasing step time in µs</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

Prepares the specified DDS channel for a frequency ramp by loading the specified ramp generation parameters and enabling the ramp with frequency set as the destination parameter. The amplitude and phase offset parameters are determined by the currently active single-tone profile.

### DDS Set Phase Ramp

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref in</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>channel number</td>
<td>unsigned byte</td>
<td>the channel (1–4) to set</td>
</tr>
<tr>
<td>ramping pattern</td>
<td>Digital ramping pattern</td>
<td></td>
</tr>
<tr>
<td>high phase offset</td>
<td>double</td>
<td>ramp upper limit phase offset in radians</td>
</tr>
<tr>
<td>low phase offset</td>
<td>double</td>
<td>ramp lower limit phase offset in radians</td>
</tr>
<tr>
<td>positive phase step</td>
<td>double</td>
<td>increasing phase step in radians</td>
</tr>
<tr>
<td>negative phase step</td>
<td>double</td>
<td>decreasing phase step in radians</td>
</tr>
<tr>
<td>pos ramp step time</td>
<td>double</td>
<td>increasing step time in µs</td>
</tr>
<tr>
<td>neg ramp step time</td>
<td>double</td>
<td>decreasing step time in µs</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

Prepares the specified DDS channel for a ramp of the phase offset of the RF output by loading the specified ramp generation parameters and enabling the ramp with phase set as the destination parameter. The frequency and amplitude parameters are determined by the currently active single-tone profile.
CHAPTER 8. LABVIEW PROGRAMMING INTERFACE

DDS Set Single-Tone Profile

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref in channel number</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>profile</td>
<td>unsigned byte</td>
<td>the channel (1–4) to set</td>
</tr>
<tr>
<td>frequency</td>
<td>unsigned byte</td>
<td>the profile number (0–7) to set</td>
</tr>
<tr>
<td>phase offset</td>
<td>double</td>
<td>the frequency to load in MHz</td>
</tr>
<tr>
<td>amplitude</td>
<td>double</td>
<td>the phase offset to load in radians</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

Loads the RF generation parameters of amplitude, phase offset, and frequency into the given single-tone profile of the given channel.

DDS Wake Up

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref in channel number</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>error in</td>
<td>unsigned byte</td>
<td>the channel (1–4) to wake</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

Wakes up the specified channel from a DDS Power Down command, restoring its previous state without erasing data.

DDS Write Register

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDS ref in channel number</td>
<td>DDS box device reference</td>
<td></td>
</tr>
<tr>
<td>register</td>
<td>unsigned byte</td>
<td>the channel (1–4) to load into</td>
</tr>
<tr>
<td>write data</td>
<td>AD9910 registers</td>
<td>the register to load into</td>
</tr>
<tr>
<td>write data</td>
<td>1-D array of unsigned byte</td>
<td>the data to upload</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

Writes data to the specified register in the specified channel. The number of bytes written must equal the register size in bytes (see the register map).
and bit descriptions section of the AD9910 data sheet for more information on registers).

8.3 Useful Sub-VIs

**DDS Pulse IO Reset**

<table>
<thead>
<tr>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs</td>
<td></td>
</tr>
<tr>
<td>spi script reference in</td>
<td>refnum</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
</tr>
<tr>
<td>Outputs</td>
<td></td>
</tr>
<tr>
<td>spi script reference out</td>
<td>refnum</td>
</tr>
<tr>
<td>error out</td>
<td>error cluster</td>
</tr>
</tbody>
</table>

This VI must be used as part of an NI-845x SPI script.

Issues a pulse to the IO Reset pin of all channels (currently one of the extra CS pins of the USB-8451). This clears the serial communication buffer of the AD9910 and readies it for a new data transmission. The IO Reset pins of all channels are physically connected via the IO board. It is not a problem that all channels share this signal since it does not directly affect the contents of chip memory, and only one channel communicates with the computer at a time.

**DDS Pulse IO Update**

<table>
<thead>
<tr>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inputs</td>
<td></td>
</tr>
<tr>
<td>spi script reference in</td>
<td>refnum</td>
</tr>
<tr>
<td>port number</td>
<td>unsigned byte</td>
</tr>
<tr>
<td>channel number</td>
<td>unsigned byte</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
</tr>
<tr>
<td>Outputs</td>
<td></td>
</tr>
<tr>
<td>spi script reference out</td>
<td>refnum</td>
</tr>
<tr>
<td>error out</td>
<td>error cluster</td>
</tr>
</tbody>
</table>

This VI must be used as part of an NI-845x SPI script.

Issues a pulse to the IO Update pin of the specified channel (currently a DIO pin of the USB-8451). An IO Update pulse signals the AD9910 to transfer data from the serial buffer to memory. See the serial programming section of the AD9910 data sheet for more information.
DDS Pulse Master Reset

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Type</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>spi script reference in</td>
<td>refnum</td>
<td>port number of the master reset pin</td>
</tr>
<tr>
<td>port number</td>
<td>unsigned byte</td>
<td></td>
</tr>
<tr>
<td>channel number</td>
<td>unsigned byte</td>
<td>the channel (1–4) to pulse</td>
</tr>
<tr>
<td>error in</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Outputs</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>spi script reference out</td>
<td>refnum</td>
<td></td>
</tr>
<tr>
<td>error out</td>
<td>error cluster</td>
<td></td>
</tr>
</tbody>
</table>

This VI must be used as part of an NI-845x SPI script.

Issues a pulse to the Master Reset pin of the specified channel (currently a DIO pin of the USB-8451). This returns the AD9910 to its default state, clearing all user data uploaded to the registers since the last reset pulse. Note that in the reset state the register settings of the AD9910 are not suitable for use in the DDS box; they must be reinitialized after a reset pulse.
9 Extending the code

If a hardware change ever necessitates a re-shuffling of the CS and DIO pin assignments of the USB-8451, first make the necessary changes in the DDS **CS pins** and **DDS DIO pins** type definitions. If no assignments need to be switched from a CS pin to a DIO pin or vice versa, then nothing else needs to be done. Otherwise update the sub-VIs described in section 8.3 to reflect the changes.

The current hardware setup should be sufficient to access the RAM modulation mode function of the AD9910. The only external pin needed to trigger RAM sweeps is IO update, which is already accessible from the DDS box front panel. The programming for RAM modulation mode should be similar to that for digital ramping: pre-load user data through the serial port, then enable the mode in the control registers.

If the DDS box hardware is modified to enable parallel data port modulation, then the serial port will be needed first to initialize parallel data port modulation mode. Most of the work required to implement this mode, however, will involve the communication protocol between the chip and the fast electronics that will be used to control the parallel data lines.